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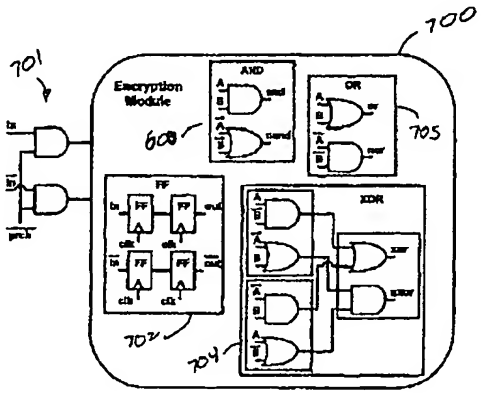
(54) Title: LOGIC SYSTEM FOR DPA AND/OR SIDE CHANNEL ATTACK RESISTANCE



(57) Abstract: DPA resistant logic circuits and routing are described. An architecture and methodology are suitable for integration in a common automated EDA design tool flow. The architecture and design methodology can be used in logic circuits, gate arrays, FPGAs, cryptographic processors, etc. In one embodiment, the implementation details of how to create a secure encryption module can be hidden from the designer. The designer is thus, able to write the code for the design of DPA resistant logic circuits using the same design techniques used for conventional logic circuits. Contrary to other complicated DPA blocking techniques, the designer does not need specialized knowledge and understanding of the methodology. In one embodiment, the automated design flow generates a secure design from a Verilog or VHDL netlist. The resulting encryption module has a relatively constant power consumption that does not depend on the input signals and is thus relatively independent of which logic operations are performed. In one embodiment, the present design methodology uses existing resources and as a result can be readily applied. In one embodiment, the architecture and design methodology blocks DPA at the logic level, freeing the designer to concentrate on preventing other side channels at a different level of abstraction (e.g., conditional branching with unequal lengths, etc.)

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